Introduction to Digital Systems

ECE 09.241

**Spring 2022**

**All Sections (1-4)**

**Instructor:** Prof. Gina Tang and Prof. Russell Trafford

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**Class Meeting:**  **Section 1:** Wednesday 1230-1345 ENGR 319

**Section 2:** Monday 1230-1345 ENGR 340

**Section 3:** Monday 1400-1515 ENGR 340

**Section 4:** Monday 1530-1645 ENGR 340

**Lab Meeting:** **Section 1:** Wednesday 1400-1645 ENGR 341

**Section 2:** Tuesday 1530-1815 ENGR 340

**Section 3:** Monday 1700-1945 ENGR 339

**Section 4:** Wednesday 1700-1945 ENGR 339

**(Optional) Kick-Off Mega Lecture:**

**All Sections:** Thursday 1530-1645 Online (Zoom)

**Office Hours: RT:** Monday 0930-1030, Wednesday 1100-1200, Appointment

**GT:** By Appointment Only

**Prerequisites:** ECE 09.101: Solving Tomorrow’s Problems

CS 04.103 or CS 04.113

**Required Material:** *zyBook Digital Design*, Vahid, Lysecky, 2021

1. Sign in or create an account at learn.zybooks.com

2. Enter zyBook code: ROWANECE09241Spring2022

3. **Select the section you are in!**

4. Subscribe

**Reference Texts:** Logic and Computer Design Fundamentals 4th Edition, Mano and Kime

**Course Attribute:** This class is one of the required core courses of the ECE curriculum. You will need a minimum of a C- to continue in the CE Sequence within ECE.

# About This class & Objectives

Digital systems dominate the globe, from a simple stopwatch to a cellphone to the international space station, each of these are dependent on digital systems. Digital systems, at the most elementary level, are composed of 0's and 1's and rudimentary logic functions. This core course takes a hands-on approach, starting with how to physically build basic logic functions (AND, OR, NOT) from transistors all the way to how to combine these functions to make complex digital systems. During the course students will learn how numbers and information are stored and manipulated in a digital system and how these basic principles can be expanded and extended to create a computer processor. The focus of the course will be on alternative number systems (Binary, Octal, Hexadecimal), Boolean algebra, minimization, combinational circuit design, and sequential circuit design. Both synchronous and asynchronous network design and state machines will be covered. Students will get hands on experience using modern development tools to design, test, and implement digital systems.

# Notes about Lecture Style

**Co-Teaching**

This semester we will co-teaching sections 2, 3, and 4 of the course. What this means is the Prof. Tang will be facilitating the Class Meetings while Prof. Trafford will be facilitating the Lab Meetings for these sections. Section 1 will be taught entirely by Prof. Trafford. This is to let us best create environments for you all to learn in with regards to what each type of meeting is about.

**“Flipped” Class**

This semester we will also be “flipping” the class a bit. In education-speak, when we say “flip” there are a lot of thoughts along the lines of “well my instructors aren’t going to do anything and I am just going to be learning on my own.” This is not what we are doing. This semester, IDS is 1 Lecture and due to the nature of the material, we felt like trying to cram in material in one, 75-minute session just doesn’t work. Instead we wanted to focus on how to **best utilize your limited in-class time** and from several years and different courses worth of feedback, time and time again, one of the most valuable things if going over and practicing applying the material.

What this means that the “Lectures”, which we are calling “Class Meetings” are going to be revolving around solving problems and reviewing material. The is essentially meant to take place in the **middle** of your learning. For most of your life, lecture classes have been the beginning of new material, and we want to call this out because if you approach this class normally, you are going to struggle quite a bit. Class meetings will **assume** you have done the reading and learning for the week before coming in. This lets us do practice problems and focus on confusion points or areas which may need a little more explanation. If you are not proactive and do not learn before coming to the Class Meetings, **you will most likely not pass this class**.

**Kick-Off Mega Lecture**

Since this is going to be a departure from what you are used to, for those who still would like to hear a lecture will be given the opportunity. Each week on **Thursday from 1530-1645** will be the Kick-Off for the new material in the course. This day picked for several reasons:

* Thursday means you will have about 3-4 days to review and learn the material for the following week. Then you can discuss and review in the Class Meetings.
* Thursday is a time which works for our instructor schedules.
* This timeslot is also a time where, COVID-19 allowing, we could potentially lecture in the Rowan Lecture Hall.

*Is listening to this lecture a substitute for your own learning?* **NO**. This is meant to let you see the topics discussed at a very very high level and to introduce the ideas to you. You still need to do your own learning.

*If I cannot make it, am I doomed?* **NO.** The benefit to doing this type of lecture remotely and on Zoom is we can easily record it and make it available for everyone to see and go back to.

# Course Outcomes & Performance Indicators

Upon successful completion of this class, you will be able to design and implement digital systems for a broad spectrum of real-world problems and applications.

The following general performance indicators will be used to assess whether you and this class have met the course objectives and outcomes.

* Convert between Decimal, Binary, Octal, and Hexadecimal number systems and perform basic base-n arithmetic.
* Design and optimize combinational logic circuits using Boolean algebra, truth tables, K-maps, etc.
* Build logic gates from discrete MOSFETs and build circuits from discrete logic gates.
* Create sequential circuits, state machines, Mealy-machine, Moore-machine, etc.
* Design digital circuits on a FPGA using Verilog HDL and logic schematics.

## **ABET Criteria (Student Outcomes) Met by This Course**

The outcomes of this course – assessed by a combination of in class review orals, midterm and final exams, weekly laboratory design exercises, and final design project, as well as attendance and professionalism – meet the following ABET criteria

1. an ability to apply knowledge of mathematics, science, and engineering

PI 1: Students can design and optimize combinational logic circuits using Boolean algebra, truth tables, K-maps, etc.

PI 2: Students can convert between Decimal, Binary, Octal, and Hexadecimal number systems and perform basic base-n arithmetic

1. an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.

PI 1: Students can build logic gates from discrete MOSFETs and build circuits from discrete logic gates.

PI 2: Students can create sequential circuits, state machines, Mealy-machine, Moore-machine, etc.

1. an ability to identify, formulate, and solve engineering problems

PI 1: Students can do high-level design using state-machines, Mealy-machine, Moore-machine, etc.

PI 2: Students can formulate the practical real-world problems in mathematical (Boolean algebraic) language.

1. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

PI 1: Students can design digital circuits on a FPGA using Verilog HDL and logic schematics.

**Course Prerequisites**

ECE 09.101: Solving Tomorrow’s Problems

Dependent Topics:

* General Programming Ideology
* Microcontroller Usage
* Digital Logic Introductions

CS 04.103 or CS 04.113

Dependent Topics:

* Programming Structure
* Conditionals, Loops
* Variables, Value Representation
* General Software Design

**Attendance Policy**

Attendance is expected.

**Grading Scale**

An *absolute* grading scheme will be used to assess your final grade:

Weekly Quizzes: 15%

Assignments: 10%

Exams : 30%

Labs: 30%  
 Final Project: 15%

*Professionalism, good academic citizenship, professional and ethical conduct, and active class participation are expected.*

# Course Content

* **Week 1** 
  + **Topics:** Basic Logic Gates,Number Bases, Boolean Math Expressions, Boolean Algebra Identities (No Demorgans)
  + **Assignment 1 -** Read and complete Week 1 in Zybooks
  + **Lab 0 -** Introduction to the DE0 and Altera Design Software
* **Week 2**
  + **Topics:** Minterms, Maxterms, Standard Forms, Demorgans, K-Maps
  + **Assignment 2 -** Read and complete Week 2 in Zybooks
  + **Lab 1** - Designing and Implementing 7-Segment Decoders
* **Week 3**
  + **Topics:** Encoders/Decoders, Muxes, Dont Cares, Verilog.
  + **Assignment 3 -** Read and complete Week 3 in Zybooks
  + **Lab 2** - Multiple Selection Display (Structural and Dataflow Tutorial), Testbench Example
* **Week 4**
  + **Topics:** SR-Latches, Flip-Flops, Registers, Clocks
  + **Assignment 4 -** Read and complete Week 4 in Zybooks
  + **Lab 3** - 6-Digit Display with Memory, and testbench design
* **Week 5**
  + **Topics:** State Diagrams, Parts of a state machine, describing behavior of FSMs, FSM Circuits
  + **Assignment 5 -** Read and complete Week 5 in Zybooks
  + **Lab 4** - Sequence Recognizer and Physically Building a FSM
* **Week 6**
  + **Topics:** Creating Sequential Circuits from FSMs, State Reduction, State Encoding
  + **Assignment 6 -** Read and complete Week 6 in Zybooks
  + **Lab 5** - Gridlock
* **Week 7**
  + **Topics:** Mealy Machines and Actions, Issues with FSMs
  + **Assignment 7 -** Read and complete Week 7 in Zybooks
  + **Lab 6** - Integrating Left Turn Lights and Crosswalks
* **Week 8**
  + **Topics:** Adders, Two’s Compliment, Substractors, Comparators
  + **Assignment 8 -** Read and complete Week 8 in Zybooks
  + **Lab 7** - TBD
* **Week 9**
  + **Topics:** N-Bit Muxes, Load Registers, Shifters, Counters, Timers
  + **Assignment 9 -** Read and complete Week 9 in Zybooks
  + **Lab 8** - TBD
* **Week 10**
  + **Topics:** High-Level State Machines, Variables, Loops
  + **Assignment 10 -** Read and complete Week 10 in Zybooks
  + **Lab 9** - TBD
* **Week 11**
  + **Topics:** HLSM Datapaths and RTL Design
  + **Assignment 11 -** Read and Complete Week 11 in Zybooks
  + **Lab 10** - Final Project
* **Week 12**
  + **Topics:** Advanced Datapath Components
  + **Assignment 12 -** Read and complete Week 12 in Zybooks
  + **Lab 11** - Final Project
* **Week 13**
  + **Topics:** Multi-Function Registers and ALUs
  + **Assignment 13 -** Read and complete Week 13 in Zybooks
  + **Lab 12** - Final Project
* **Week 14**
  + **Topics:** Memory Architectures
  + **Assignment 14 -** Read and complete Week 14 in Zybooks
  + **Lab 13** - Final Project

# Accommodation for Disability & Academic Success Center

If you have a documented physical and/or learning disability, please inform the Academic Success Center (ACS; director: John Woodruff – [woodruff@rowan.edu](mailto:woodruff@rowan.edu), or 856-256-4234) regarding what kind of accommodation you need to help you succeed in this class. While you are not required to disclose details of your disability to me, you must provide appropriate documentation to the ACS to receive official university assistance. I can only provide special accommodation if I receive a letter describing the nature of such accommodation from the ACS. Accommodation requests without a letter from ACS cannot be honored. All such requests will be held confidential to the extent possible. Please visit the following page for additional details and instructions: <http://www.rowan.edu/studentaffairs/asc/disabilityresources/> .

Academic success center also provides a variety of other services, including tutoring services, which are all typically free. I encourage you to take advantage of these services. Please contact them at 304 Savitz Hall, or by visiting their website at <http://www.rowan.edu/studentaffairs/asc/>

You may also be interested in the Rowan Success Network, designed to make it easier for you to connect with the resources you need to be successful at Rowan. Throughout the term, you may receive email from the Rowan Success Network team (Starfish®) regarding your academic performance. Please pay attention to these emails and consider taking the recommended actions. Utilize the scheduling tools to make appointments at your convenience including tutoring. Additional information about RSN may be found at [www.rowan.edu/rsn](http://www.rowan.edu/rsn).

# ACADEMIC DISHONESTY POLICY

Academic dishonesty, in all forms – including but not limited to plagiarism – will not be tolerated. In general, any attempt to represent somebody else’s work as if it is yours is considered plagiarism. Please note that aiding or assisting another student to commit plagiarism is itself academic dishonesty as well. All cases of academic integrity violations will be reported to the Provost’s Office and will be dealt with as described in the [Rowan University Academic Integrity Policy](https://confluence.rowan.edu/display/POLICY/Academic+Integrity+Policy).